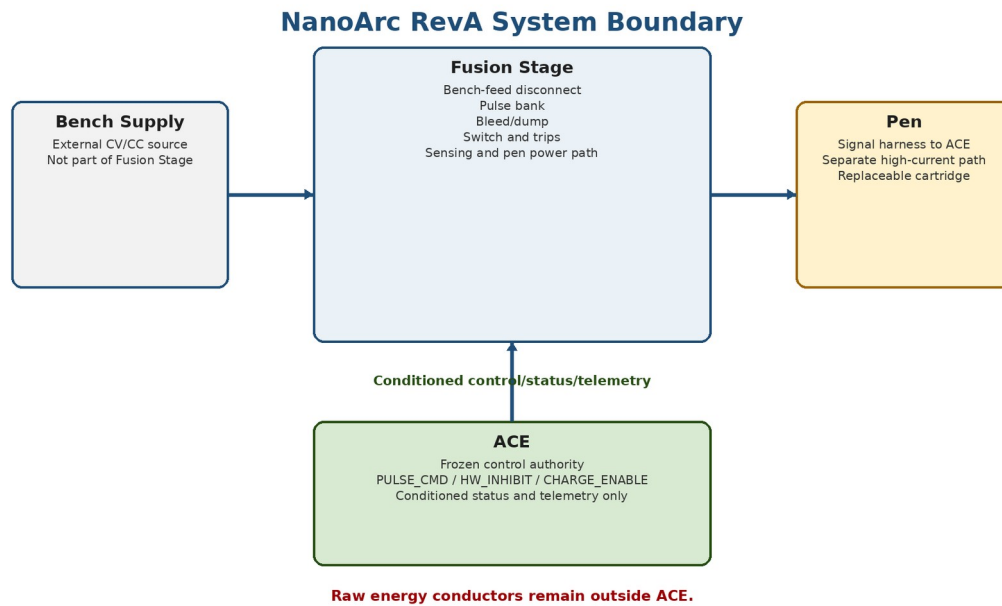


NANOARC

Fusion Stage Technical Specification

Revision A.0 - Architecture, Interface, Requirements and Verification Baseline



Field	Value
Document identifier	NA-FUSION-001
Revision	A.0 working draft
Date	2026-07-01
Status	Architecture and requirements baseline - parameters pending characterization
Authority	Subordinate to NA-MASTER-001 RevA Freeze / Master Revision 1.2
Scope	Bench-fed pulse bank, switch stage, sensing, protection, output harness and pen
Controller relationship	ACE is frozen and is the sole positive pulse authority

DESIGN NOTE: This document defines how the Fusion Stage shall work in harmony with the frozen ACE module. It does not authorize changes to ACE hardware, pin ownership, firmware architecture or operator semantics.

Document Control and Revision Record

Revision	Date	Status	Summary
A.0	2026-07-01	Working draft	Initial integrated Fusion Stage architecture, ACE interface constraints, subsystem requirements and verification baseline.
A.1	Reserved	Future controlled issue	Freeze characterized electrical ranges, selected components, thresholds, cable geometry and acceptance limits.
B	Reserved	Future integration revision	Portable source, production harnessing and consolidated machine I/O only after RevA evidence.

CONFIGURATION PRECEDENCE: NA-MASTER-001 Part I remains the highest-authority NanoArc document. This specification may refine only the external machine implementation behind the frozen ACE contracts. Any conflict is resolved in favour of NA-MASTER-001.

Status Vocabulary

Status	Meaning
Frozen	Required by the ACE master baseline or explicitly adopted here.
Proposed	Preferred architecture pending review.
TBD	A value or implementation must be established by characterization.
DNP	Reserved but not populated in the present revision.
Non-normative	Historical concept retained only for traceability.

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1. Purpose, Scope and Authority

This specification defines the NanoArc RevA Fusion Stage: the bench-fed, low-voltage energy-storage and pulse-delivery hardware controlled by ACE. It establishes subsystem boundaries, interface behaviour, safety relationships, sensing, handpiece functions, verification evidence and the process for freezing the remaining electrical parameters.

The Fusion Stage is analogous to a controlled machine attachment. ACE remains the supervisory computer and the only source of positive pulse authorization. The Fusion Stage shall convert an accepted ACE command into a bounded electrical pulse, report what physically occurred, and preserve or reduce authorization when faults are detected.

SCOPE LIMIT: This revision begins at the external bench supply output terminals. The bench supply, internal mains conversion, battery pack, BMS, portable charger, USB-C PD and any boost/buck charging converter are outside RevA scope.

2. Configuration Precedence and Compatibility Rule

The controlling precedence is: (1) NA-MASTER-001 Part I; (2) approved engineering change orders; (3) aligned ACE component manuals; (4) this Fusion Stage specification; and (5) historical brainstorming notes. Historical 40 V, 10 J, USB-C, STM32 and local-display concepts are non-normative and may not override the current ACE baseline.

PRIMARY RULE: ACE defines the interface. The Fusion Stage implements the machine behind that interface.

- No new mandatory ACE direct pin may be introduced by this document.
- No ACE direct pin may be reassigned, inverted or repurposed.
- No raw energy-stage node may enter ACE or the operator panel.
- No local Fusion Stage control may bypass PULSE_CMD or HW_INHIBIT.
- Any connector shell or keying decision must preserve the frozen functional segregation.

3. Product Mission and Use Cases

NanoArc is a precision capacitor-discharge micro-bonding tool for localized work on small electronic assemblies and thin conductive materials. RevA is a characterization platform as well as a usable engineering prototype; its architecture shall permit controlled substitution of the bank, switch cartridge, output cable and electrode cartridge without changing ACE.

3.1 Primary Mission

- Localized solder-paste heating on small PCB pads and header joints.
- Repair or attachment of thin conductive foils and small contacts.
- Repeatable single operations supervised by ACE P10 and bounded repeat sessions under P11.
- Instrumented characterization of energy, current, temperature, contact and joint response.

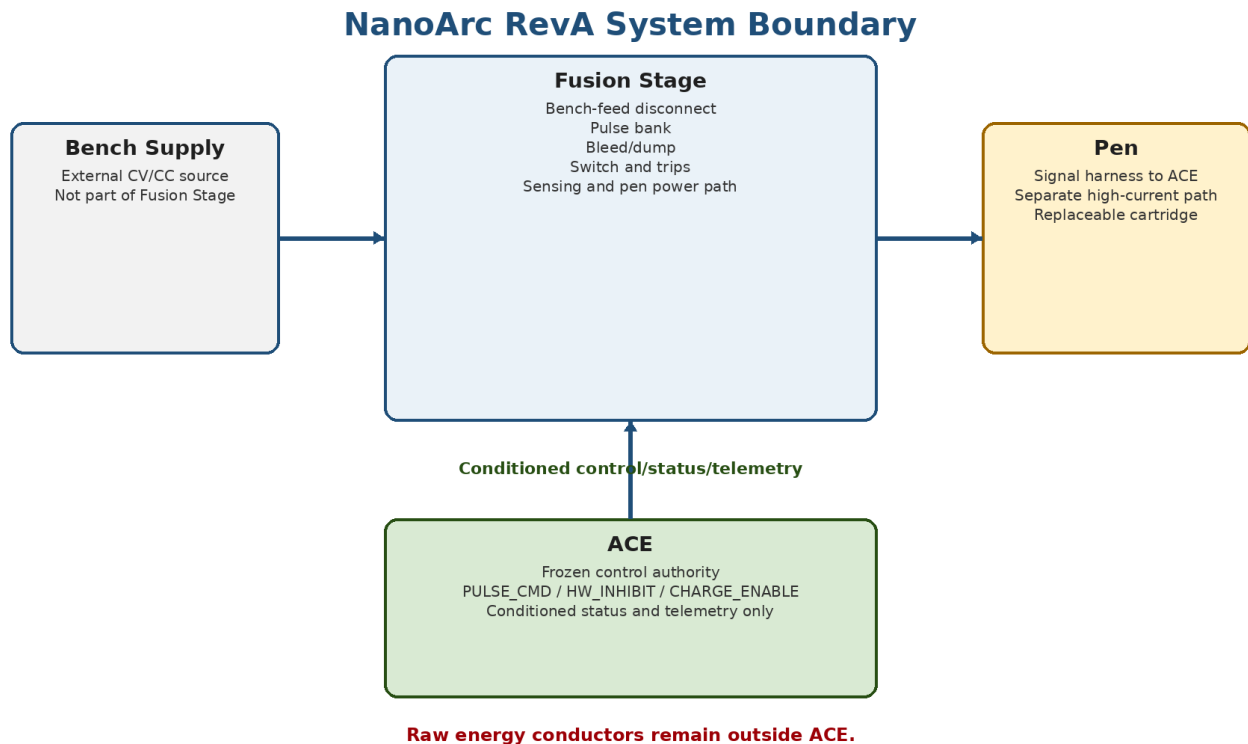
3.2 Out-of-Scope Mission

- Structural welding, thick sheet welding or continuous-duty industrial operation.
- Large-format battery-tab production or unattended automated cycling.
- Operation without the verified ACE authorization and inhibit chain.
- Use of the bench source as the direct pulse source without the defined bank and switch controls.

4. Terminology and Abbreviations

Term	Definition
ACE	NanoArc control electronics; the frozen sole positive pulse authority.
Fusion Stage	The external machine hardware that stores and delivers the pulse and reports conditioned facts to ACE.
Positive authority	The ability to initiate an output. Only ACE possesses positive pulse authority.
Negative authority	The ability to block or terminate an output. Independent safety hardware possesses negative authority only.
Preparation	Bench-source-to-bank feed activity requested by CHARGE_ENABLE while output remains inhibited.
Pulse bank	Energy-storage capacitor assembly and its mechanical/electrical support.
Power cartridge	Replaceable high-current portion of the pen, including electrode holders and electrodes.
Fresh trigger	A new transition from released to pressed after ACE has entered an eligible ready condition.
Conditioned fact	A protected, scaled or logic-level signal suitable for ACE.
Raw node	An energy-storage, busbar, shunt, electrode or pulse-current node prohibited from entering ACE.

5. System Boundary



The external bench source provides regulated voltage and current limitation. FS-100 decides whether the bank may be connected to that source. FS-200 stores energy and manages residual charge. FS-300 accepts the bounded ACE pulse request through independent veto logic. FS-400 and FS-500 carry the pulse to the workpiece. FS-600 through FS-800 provide measurements, trips and conditioned interfaces.

BOUNDARY: The Fusion Stage starts at the bench-source input connector and ends at the electrode/workpiece interface. ACE and the bench supply are adjacent systems, not Fusion Stage subassemblies.

6. Frozen ACE Compatibility Invariants

- PULSE_CMD is the timer-owned bounded request generated by ACE.
- HW_INHIBIT is dominant safe and shall be effective during reset, wiring loss and undefined state.
- CHARGE_ENABLE is a supervised preparation request, inactive on reset.
- FAULT_SUM, TRIP_OV, TRIP_OC and OUTPUT_FB are direct conditioned facts.
- GRIP_SW, TRIGGER_SW and HANDPIECE_PRESENT are direct ACE inputs.
- No Class-A signal is mediated solely by I2C or a Fusion Stage software process.
- ACE may observe, diagnose and log; independent trips shall already have removed the output path.

ID	Title	Requirement	Verification	Status
FS-ACE-001	Sole pulse authority	Only ACE PULSE_CMD may initiate conduction in the output switch stage.	Test	Frozen
FS-ACE-002	Dominant inhibit	Active HW_INHIBIT shall prevent or terminate gate drive regardless of PULSE_CMD state.	Fault injection	Frozen
FS-ACE-003	No trigger bypass	No electrical path from pen trigger or grip shall directly drive the Fusion Stage output switch.	Inspection/Test	Frozen
FS-ACE-004	No pulse memory	The Fusion Stage shall not store a pending pulse request after PULSE_CMD is removed.	Test	Frozen
FS-ACE-005	No autonomous retrigger	The Fusion Stage shall not generate repeated or extended pulses from a single ACE command.	Test	Frozen
FS-ACE-006	Open wiring safe	Open or disconnected ACE control wiring shall resolve to inhibited/unavailable states.	Fault injection	Frozen

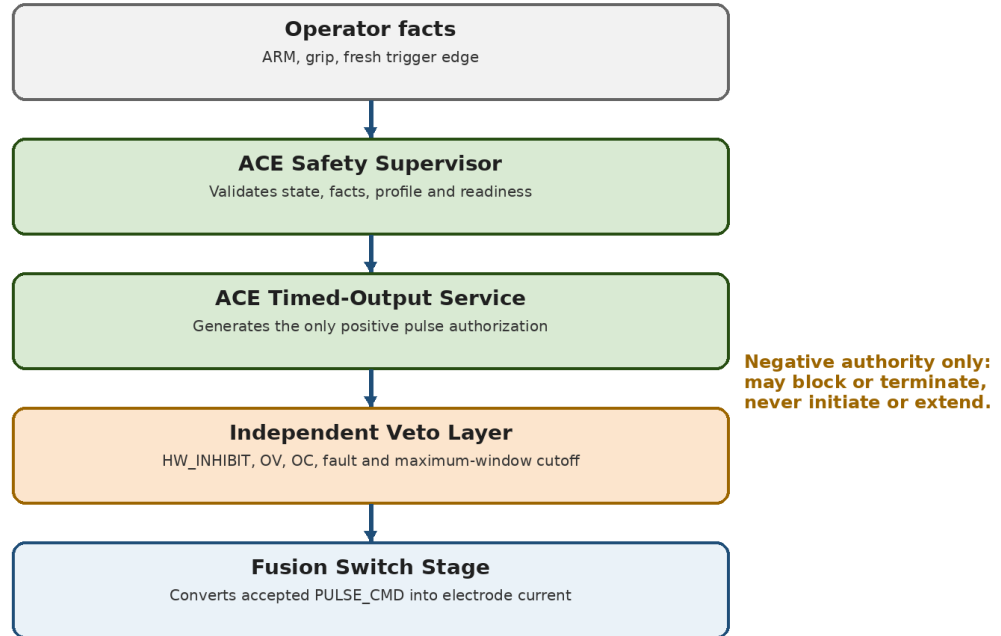
7. Operating Concept

1. The bench source is connected and configured within the characterized RevA envelope.
2. ACE remains inhibited while the Fusion Stage proves presence, safe defaults and valid telemetry.
3. ACE requests preparation using CHARGE_ENABLE; FS-100 connects the bench source to the bank only while permitted.
4. FS-200 reports bank voltage, charge current and temperature. Independent overvoltage hardware remains authoritative.
5. ACE removes preparation and evaluates readiness, handpiece identity, physical ARM, grip and a fresh trigger request.
6. ACE releases the output window and generates PULSE_CMD through its timed-output service.
7. FS-300 conducts only while PULSE_CMD is present and every independent veto remains clear.

8. OUTPUT_FB and current telemetry report the physical result; any mismatch or trip forces inhibit.
9. ACE reasserts inhibit, evaluates cooldown/readiness and requires trigger release before another operation.

8. Authority and Trigger Model

Pulse Authority and Veto Chain



The pen button is a request to ACE, not a gate-drive path.

8.1 Positive Authority

ACE alone determines whether the machine is ready, whether the operator request is acceptable and how long the output request remains active. The pen button is a direct request fact to ACE. It is not an electrical enable for the gate driver.

8.2 Negative Authority

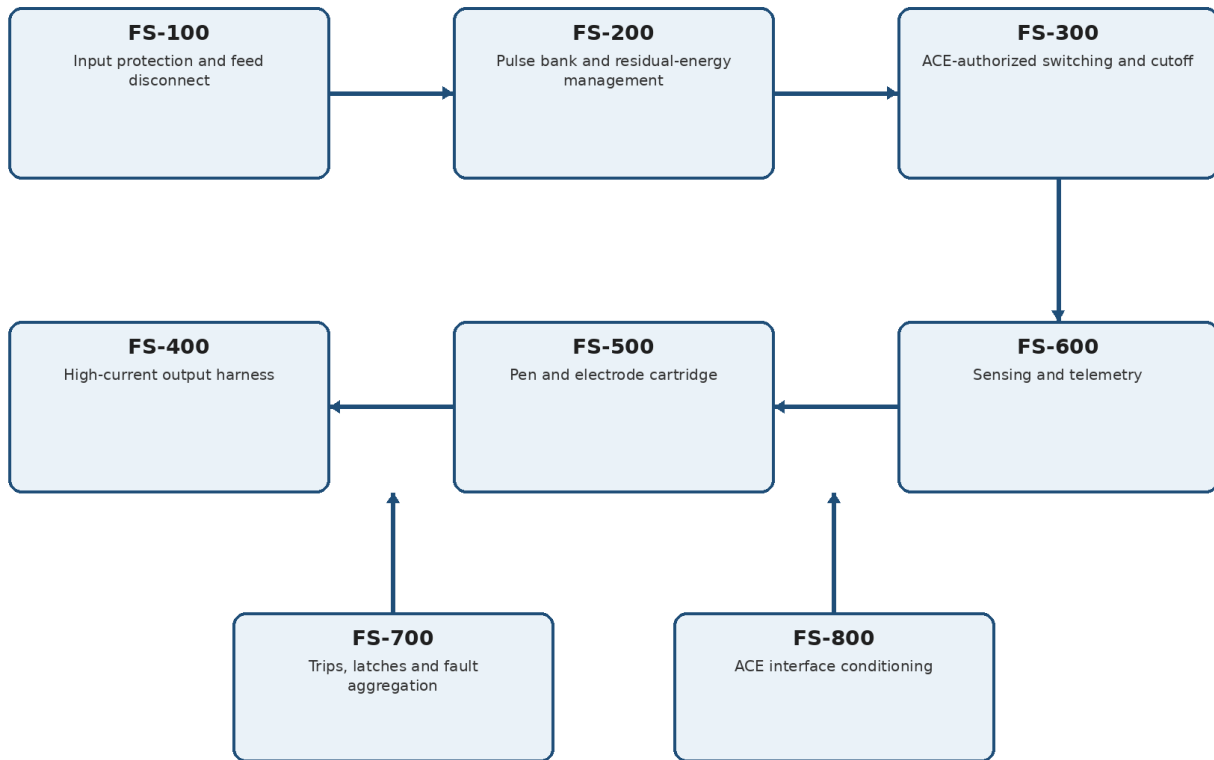
The Fusion Stage may block or terminate conduction in response to HW_INHIBIT, independent overvoltage, independent overcurrent, aggregate fault, pulse-clamp expiry, invalid local supply or other frozen veto. These conditions do not become alternate positive authorities.

Condition	Effect
PULSE_CMD inactive	Gate drive off.
HW_INHIBIT active	Gate drive off; feed disconnect safe.
TRIP_OV active	Preparation and output blocked; fault latched.
TRIP_OC active	Output terminated; fault latched.
FAULT_SUM active	Output blocked or terminated.
Clamp expired	Output terminated; fault source recorded.
Control harness absent	Output and preparation disabled.

Condition	Effect
Reset/brownout	Output and preparation disabled by hardware defaults.

9. Functional Architecture

Fusion Stage Functional Partition



Module	Primary responsibility	ACE-facing products
FS-100	Input protection, source presence and controlled bank feed.	VIN_AUX, ICHG_MON, CHARGER_READY, CHARGER_FAULT.
FS-200	Energy storage, bank structure, passive bleed and active dump.	VBANK, TBANK, BLEED_CONFIRM.
FS-300	Pulse switching, gate drive and output-state observation.	PULSE_CMD input, HW_INHIBIT input, OUTPUT_FB output.
FS-400	High-current output connector, cable and return loop.	IOUT_MON and physical output path.
FS-500	Pen body, signal inputs, tool identity, temperature and electrode cartridge.	GRIP_SW, TRIGGER_SW, HANDPIECE_PRESENT, THAND, HANDPIECE_ID.
FS-600	Analog scaling, filtering, validity and sensor conditioning.	Defined ADC channels.
FS-700	OV/OC/thermal/window trips, source latch and FAULT_SUM.	TRIP_OV, TRIP_OC, FAULT_SUM, FAULT_LATCH_VALID.
FS-800	Connector protection, level conditioning, returns and segregation.	J-PWR, J-HND and J-AUX compliance.

10. ACE Interface Contract

10.1 Direct Signals

Signal	Direction	Fusion Stage obligation
FAULT_SUM	Fusion -> ACE	Open-drain aggregate critical fault; safe/unavailable when open wiring is detected by the ACE-side contract.
TRIP_OV	Fusion -> ACE	Independent bank overvoltage comparator fact.
TRIP_OC	Fusion -> ACE	Independent pulse-current trip fact.
OUTPUT_FB	Fusion -> ACE	Observed physical output state for command/actual cross-check.
PULSE_CMD	ACE -> Fusion	Only positive pulse authorization; bounded and timer-owned by ACE.
HW_INHIBIT	ACE -> Fusion	Dominant safe request; shall override PULSE_CMD and preparation.
CHARGE_ENABLE	ACE -> Fusion	Supervised preparation request; inactive on reset.
GRIP_SW	Pen -> ACE	Independent handpiece enabling contact.
TRIGGER_SW	Pen -> ACE	Final operator request; safe on open.
HANDPIECE_PRESENT	Pen -> ACE	Direct presence fact.

10.2 Machine I/O Functions

Function	Direction	Requirement
CHARGER_READY	Fusion -> ACE	Feed path and local preparation hardware available.
CHARGER_FAULT	Fusion -> ACE	Feed path or source-supervision fault.
BLEED_CONFIRM	Fusion -> ACE	Residual-energy management reports expected state.
FAN_TACH_OR_GOOD	Fusion -> ACE	Cooling status where fitted.
AUX_INTERLOCK	Fusion -> ACE	Additional enclosure or service interlock.
POWER_MODULE_PRESENT	Fusion -> ACE	Fusion Stage presence/identity fact.
FAULT_LATCH_VALID	Fusion -> ACE	Detailed source bitmap is valid.
BLEED_ENABLE	ACE -> Fusion	Requests active residual-energy discharge.
FAN_ENABLE	ACE -> Fusion	Requests supervised cooling.
CONTACT_TEST_ENABLE	ACE -> Fusion	Requests low-energy contact measurement.
FAULT_LATCH_RESET	ACE -> Fusion	Clears detailed source latch only when the source is absent.

10.3 Connector Functions

Connector	Baseline	Rules
J-PWR	12-circuit conditioned machine interface	Commands/status only; raw energy nodes prohibited; exact shell/keying remains change-controlled.
J-HND	8-circuit handpiece signal interface	Trigger, grip, presence, ID, temperature, shield/drain and returns only.
High-current pen connector	Separate Fusion Stage connector	No mating compatibility with J-PWR or J-HND; source side shall avoid exposed energized contacts.
J-AUX	6-circuit enclosure/service interface	Enclosure, service, fan/status and reserved functions.

11. External Bench-Source Boundary

The bench source is a development and RevA operating dependency but not part of the Fusion Stage BOM or controlled hardware. It provides adjustable CV/CC operation. The Fusion Stage shall not depend on undocumented source behaviour and shall remain safe if the source is removed, current-limits, folds back or is incorrectly connected within the protected fault assumptions.

Source attribute	Specification treatment
Nominal voltage range	TBD from bank-energy characterization; documented before energized release.
Maximum current	TBD from acceptable preparation time and feed-path thermal limits.
Current limiting	Required external capability; not replaced by Fusion Stage logic.
Output isolation/grounding	Characterized with the final bench unit and enclosure bonding plan.
Remote sense	Optional; not assumed by the Fusion Stage.
Transient behaviour	Measured during connection, disconnect, current limit and pulse exclusion.

12. FS-100 Input Protection and Feed Disconnect

FS-100 accepts the bench source, protects the Fusion Stage, measures source and charge current, and permits preparation only when CHARGE_ENABLE is valid and HW_INHIBIT is not dominant. It is not an internal charger or regulator.

ID	Title	Requirement	Verification	Status
FS-IN-001	Input fuse/protection	The input path shall include protection sized from the characterized source, wiring and credible fault current.	Analysis/Test	TBD
FS-IN-002	Controlled disconnect	A hardware-controlled feed disconnect shall isolate the bank from the bench source when CHARGE_ENABLE is inactive.	Test	Proposed
FS-IN-003	Inhibit dominance	HW_INHIBIT and critical fault conditions shall force	Fault injection	Frozen

ID	Title	Requirement	Verification	Status
		the feed disconnect safe independently of ACE software sequencing.		
FS-IN-004	Pulse exclusion	The feed path shall not conduct meaningful preparation current during the output pulse window.	Measurement	Proposed
FS-IN-005	Source telemetry	VIN_AUX and ICHG_MON shall be scaled, filtered and range-checked before ACE acquisition.	Calibration/Test	Frozen
FS-IN-006	Reverse-current behaviour	The selected feed-disconnect topology shall have documented reverse-current behaviour and shall not permit unintended bank backfeed.	Review/Test	TBD

13. FS-200 Pulse Bank

The pulse bank stores the energy commanded indirectly through ACE preparation and pulse profiles. RevA shall support characterization without forcing a redesign of ACE or the enclosure interface. Exact voltage, capacitance and energy remain open until the material and joint envelope is tested.

Parameter	RevA treatment
Maximum bank voltage	TBD; selected from the lowest practical voltage that meets the reference joint envelope.
Capacitance	TBD; derived from required energy and allowable voltage droop.
Stored energy	TBD; bounded by the primary micro-bonding mission and test evidence.
ESR/ESL	Measured as an assembled bank, not inferred solely from capacitor datasheets.
Temperature	Monitored through TBANK with independent critical threshold where required.
Mechanical mounting	Restrained, vent-aware and protected from tool/service contact.
Modularity	Bank assembly replaceable or reconfigurable during characterization.

ID	Title	Requirement	Verification	Status
FS-BANK-001	Voltage margin	Every bank component shall have rated and surge voltage margin above the characterized maximum bank voltage.	Design review	TBD
FS-BANK-002	Pulse suitability	Capacitors shall be selected using ESR, impedance, ripple, surge, lifetime and pulse-heating evidence, not capacitance and voltage alone.	Design review	TBD
FS-BANK-003	Assembled characterization	The assembled bank shall be measured for capacitance, effective series resistance, leakage, temperature rise and discharge repeatability.	Test	TBD

ID	Title	Requirement	Verification	Status
FS-BANK-004	Physical containment	Bank terminals and conductors shall be finger-safe behind tool-removable barriers in normal service states.	Inspection	Frozen
FS-BANK-005	Vent clearance	Capacitor pressure-relief vents shall not be obstructed or directed toward the operator or ACE electronics.	Inspection	Proposed
FS-BANK-006	No salvage assumption	Salvaged capacitors shall not be accepted into the released RevA configuration without measured health and traceable derating evidence.	Inspection/Test	Proposed

14. Residual-Energy Management

FS-200 shall include both a passive bleed function and an ACE-requested active dump function. These are separate safety functions: passive bleed handles loss of control power; active dump provides bounded removal of stored energy during normal inhibit, service and fault handling.

Function	Required behaviour
Passive bleed	Always connected or otherwise fail-passive; reduces bank voltage without ACE cooperation.
Active dump	Controlled by BLEED_ENABLE but available only through a hardware-safe path.
BLEED_CONFIRM	Confirms expected dump-path state or residual-energy trend; does not substitute for VBANK.
Service indication	Stored-energy status remains available through conditioned telemetry or local protected indication.
Failure response	Open, short or overtemperature conditions produce a fault or invalid fact and preserve inhibit.

15. FS-300 Pulse Switch Stage

FS-300 converts PULSE_CMD into the high-current output only while every veto condition is clear. The baseline architecture is a unidirectional low-side or otherwise equivalent switch arrangement selected for low loss, controllable gate drive and clean hardware shutdown. The final topology remains subject to layout and transient characterization.

ID	Title	Requirement	Verification	Status
FS-SW-001	Command dependence	Gate drive shall be impossible without active PULSE_CMD.	Inspection/Test	Frozen
FS-SW-002	Hardware enable chain	PULSE_CMD shall pass through hardware gating that includes HW_INHIBIT and independent trip/clamp vetoes.	Inspection/Test	Frozen
FS-SW-003	SOA-based selection	Switch devices shall be selected using safe-operating-area, transient thermal impedance, gate	Design review	TBD

ID	Title	Requirement	Verification	Status
		charge, temperature-dependent resistance and pulse repetition evidence.		
FS-SW-004	Parallel symmetry	If devices are paralleled, current path, gate impedance, thermal path and sensing shall be intentionally symmetrical.	Inspection/Measurement	TBD
FS-SW-005	Defined startup state	Gate-driver outputs shall be held off during power ramp, reset, disconnected input and undervoltage.	Test	Frozen
FS-SW-006	Output feedback	OUTPUT_FB shall report observed output conduction independently enough to detect command/actual mismatch.	Test	Frozen
FS-SW-007	Transient control	Voltage overshoot and ringing shall be measured at the assembled switch and output loop; suppression shall be selected from evidence.	Instrumented test	TBD

16. Independent Maximum-Window Clamp

The maximum-window clamp is independent of ACE firmware timing. It has negative authority only. It may shorten or terminate a pulse but may never create, retrigger or extend one. A non-retriggerable monostable or equivalent hardware is the baseline candidate.

- Triggered only by the accepted ACE output request path.
- Non-retriggerable during an active window.
- Forces gate drive off when its maximum interval expires.
- Resets to the safe state on power loss or undervoltage.
- Provides a fault source or latch indication after expiry.
- Uses a duration frozen below the damage envelope and above all valid commanded pulses.

17. Fault Detection, Latching and Aggregation

Independent hardware supervision shall assert the downstream inhibit path before ACE diagnosis. FAULT_SUM provides the immediate aggregate fact; a separate source latch preserves detailed cause information for V05 N09, P33 and service review.

Fault source	Immediate action	Recorded evidence
Bank overvoltage	Disable preparation and output.	TRIP_OV plus source latch.
Pulse overcurrent	Terminate output.	TRIP_OC plus source latch.
Output feedback mismatch	Terminate/block output.	FAULT_SUM and mismatch bit.
Maximum-window expiry	Terminate output.	Clamp-expiry source.
Critical thermal trip	Terminate/block affected function.	Thermal source and channel snapshot.
Feed-path fault	Disable preparation.	CHARGER_FAULT/source bit.
Residual-energy fault	Preserve inhibit; block service-ready.	BLEED fault/source bit.
Control/power undervoltage	Force safe outputs.	Supply/reset source where available.

18. FS-600 Sensing and Telemetry

The Fusion Stage shall provide conditioned analog measurements mapped to the frozen logical channel identifiers. Scaling, transfer functions and validity limits remain revision-specific, but the channel names and meanings are stable.

Channel	Signal	Fusion Stage measurement
AIN0	VBANK	Bank voltage; cross-checks independent overvoltage trip.
AIN1	VIN_AUX	Bench-source/input voltage.
AIN2	ICHG_MON	Preparation/charge current.
AIN3	IOUT_MON	Pulse output current from isolated Hall or characterized shunt front end.
AIN4	TBANK	Energy-storage temperature.
AIN5	TSTAGE	Switch/power-interface temperature.
AIN7	THAND	Handpiece/electrode-area temperature.
AIN9	CONTACT_TEST	Low-energy contact/continuity measurement.
AIN10	HANDPIECE_ID	Resistor-coded tool identity.
AIN11	VREF_MON	Analog-reference health.

18.1 Fact Quality

- Every channel shall expose value, validity, freshness, sequence/timestamp, source and fault quality through ACE.
- Open, short, saturation, out-of-range and unavailable conditions shall be distinguishable where practical.
- Telemetry supports supervision and diagnosis; independent hard trips remain authoritative.
- Filters shall not hide a condition that must reach a direct trip path.

19. High-Current Path and Output Harness

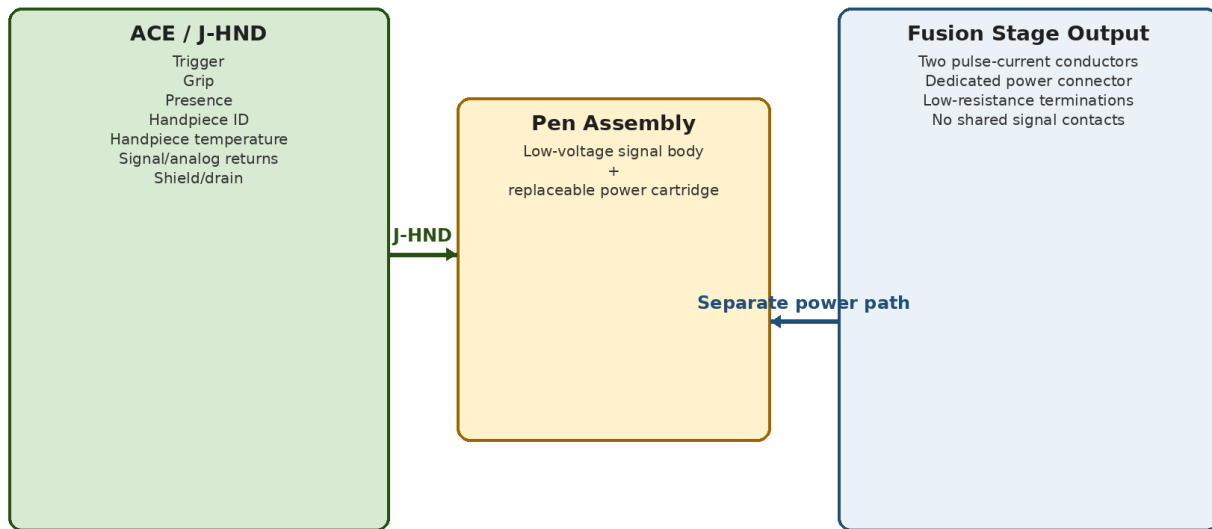
The output loop includes the bank interconnect, switch devices, current sensor, output connector, cable pair, pen conductors, electrode holders, electrodes, workpiece and return path. It shall be treated as one electrical and thermal system. The complete loop resistance and inductance determine the delivered pulse.

ID	Title	Requirement	Verification	Status
FS-PTH-001	Loop characterization	The assembled output loop shall be measured or bounded for resistance, inductance, contact resistance and temperature rise.	Measurement	TBD
FS-PTH-002	Compact internal loop	Bank-to-switch and switch-to-output conductors shall be short, mechanically restrained and arranged to minimize loop area.	Inspection/Measurement	Proposed
FS-PTH-003	No solder-only pulse joint	Primary pulse-current joints shall not rely solely on ordinary solder for mechanical retention and current transfer.	Inspection	Proposed
FS-PTH-004	Dedicated connector	The pen power connector shall be physically incompatible with ACE signal connectors and shall	Inspection	Frozen

ID	Title	Requirement	Verification	Status
		provide positive retention.		
FS-PTH-005	Source-side touch safety	The source-side output interface shall avoid exposed energized contacts in normal handling.	Inspection	Proposed
FS-PTH-006	Cable evidence	Cable selection shall use measured round-trip resistance, flex life, insulation temperature, bend radius and termination compatibility.	Design review/Test	TBD
FS-PTH-007	Strain relief	Both base and pen ends shall include strain relief that does not transfer bending load into electrical terminations.	Inspection	Proposed

20. FS-500 Pen and Electrode System

Pen Signal and Power Segregation



The high-current pen path is never part of the ACE signal connector.

20.1 Pen Architecture

The pen shall separate the low-voltage signal body from the replaceable power cartridge. The signal body contains grip, trigger, presence, identity and temperature functions. The power cartridge contains the high-current conductors, electrode holders and replaceable electrodes.

20.2 Mechanical Goals

- Pencil-like handling for PCB work without requiring the signal body to carry pulse-current joints.
- Serviceable shell and cartridge retention using mechanical fasteners or defined collets.
- Repeatable electrode spacing and projection.

- Thermal barriers between electrode holders and operator grip surfaces.
- No conductive external surface connected to the pulse path within the intended grip zone.
- Cable exit aligned to reduce wrist torque and termination fatigue.

20.3 Electrode Configurations

Configuration	Purpose	Status
Twin point - narrow	PCB/header-pitch and localized solder-paste work.	Reference candidate; spacing TBD.
Twin point - wide	Larger pads and foil coupons.	Optional cartridge.
Single point plus return clip	Constrained geometry where twin tips cannot reach.	Deferred until return-path controls are specified.
Material-specific tips	Alternate electrode materials and shapes.	Characterization option.

21. Contact Test, Tool Presence and Identity

ACE reserves a low-energy contact-test function and resistor-coded handpiece identity. These functions support readiness and configuration validation but do not become pulse authorities.

ID	Title	Requirement	Verification	Status
FS-TOOL-001	Presence fact	HANDPIECE_PRESENT shall indicate a correctly connected signal harness and shall default absent on open wiring.	Test	Frozen
FS-TOOL-002	Tool ID	HANDPIECE_ID shall use a bounded resistor-coded or equivalent passive identification method compatible with the ACE analog channel.	Calibration/Test	Frozen
FS-TOOL-003	Contact-test energy	CONTACT_TEST shall use a separately limited, low-energy measurement path incapable of generating a Fusion pulse.	Analysis/Test	Proposed
FS-TOOL-004	No auto-fire	Valid contact-test results shall be facts for ACE and shall never initiate gate drive locally.	Inspection/Test	Frozen
FS-TOOL-005	Wrong-tool inhibit	Unknown, invalid or incompatible handpiece identity shall preserve inhibit until ACE policy resolves it.	System test	Proposed

22. Thermal Management

Thermal design shall be based on the characterized pulse energy, repetition pattern, switch loss, bank ESR, connector loss and cable resistance. RevA may use passive cooling, supervised fan cooling or both. Cooling failure must reduce capability rather than create an unsafe output.

Zone	Measurement/control
Pulse bank	TBANK; vent clearance; thermal spacing from switch and enclosure walls.

Zone	Measurement/control
Switch stage	TSTAGE; heatsink or copper spreading; optional FAN_ENABLE/FAN_TACH_OR_GOOD.
Output connector/cable	Temperature rise inferred by test and inspected at terminations.
Pen/electrode mount	THAND; thermal barrier and cooldown policy.
ACE compartment	Physically separated so Fusion Stage heat and pulse currents do not compromise ACE.

23. Mechanical, Enclosure and Serviceability

- ACE and the Fusion Stage shall occupy defined low-voltage-control and energized compartments or equivalent barriers.
- Stored-energy conductors shall be covered by finger-safe barriers removable only with tools.
- Capacitors, busbars, switch modules and output connectors shall be mechanically restrained for handling and cable loads.
- Service access shall not require disturbing ACE wiring to replace a bank, switch or pen cartridge.
- Labels shall identify stored energy, bench input polarity, signal connectors, power connector and service-safe criteria.
- Enclosure interlock behaviour shall be compatible with the frozen ACE direct input and hard-safe chain.

24. EMC, Grounding and Segregation

Fast pulse currents can corrupt logic, analog measurements and fault reporting. The Fusion Stage shall be laid out as a noisy power subsystem with controlled coupling to ACE. Segregation and measurement are mandatory; no assumption of benign low voltage is acceptable for EMC.

ID	Title	Requirement	Verification	Status
FS-EMC-001	Loop-area control	Pulse-current forward and return paths shall be routed together to minimize magnetic loop area.	Inspection	Proposed
FS-EMC-002	Signal separation	J-PWR/J-HND wiring and analog sensing shall be separated from busbars, gate loops and output cable exits.	Inspection	Frozen
FS-EMC-003	Defined bonding	Chassis/shield, analog return, logic return and power return shall meet only at documented bonding points.	Inspection/Measurement	Frozen
FS-EMC-004	Connector protection	Protection components shall be located at harness entries rather than deep inside the board.	Inspection	Frozen
FS-EMC-005	Gate-loop control	Gate-driver supply, gate return and switching loops shall be compact and measured for ringing.	Inspection/Test	TBD
FS-EMC-006	Telemetry validity	Pulse activity shall not create undetected false-ready, false-trigger, false-presence or false-safe facts.	EMC/system test	Frozen

25. Diagnostics and Service

ACE P12, P30, P32 and P33 provide the primary diagnostic framework. The Fusion Stage shall expose enough conditioned facts to exercise the interface without requiring energized pulses. Critical outputs remain independently inhibited during diagnostic modes.

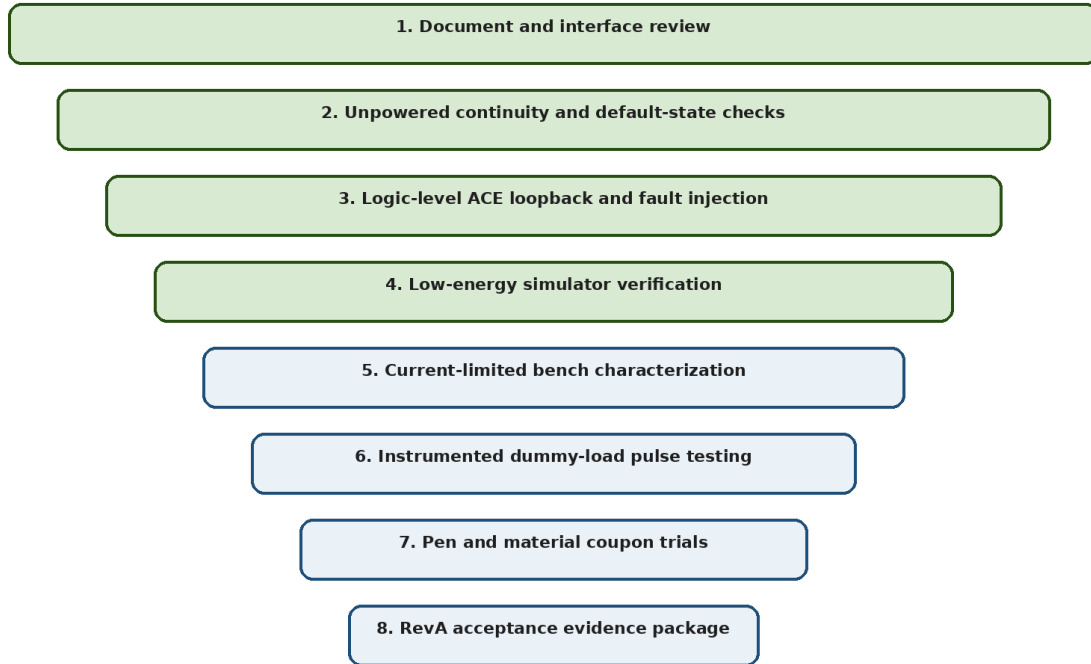
Diagnostic function	Fusion Stage support
Presence/identity	POWER_MODULE_PRESENT and HANDPIECE_PRESENT/HANDPIECE_ID.
Direct input loopback	FAULT_SUM, TRIP_OV, TRIP_OC and OUTPUT_FB test fixtures or bounded stimulus.
Machine I/O	Charger, bleed, fan, contact-test and latch controls observable without pulse output.
Analog simulation	Known test inputs or service points for VBANK, currents and temperatures.
Fault-source review	Latched source bitmap and valid flag.
Build/configuration identity	Marked module revision, populated options and calibration record.

26. Failure Behaviour and Reliability

Failure or uncertainty	Required outcome
ACE reset or brownout	Output inhibited; preparation disabled; no pulse resume.
Control harness disconnected	Output inhibited; preparation disabled; required facts unavailable.
Trigger held during readiness transition	No pulse until release and a fresh press are observed by ACE.
PULSE_CMD stuck active	Independent maximum-window clamp terminates output.
Gate-driver undervoltage	Defined off state; fault or unavailable status.
OV comparator asserted	Preparation and output disabled before diagnosis.
OC comparator asserted	Output terminated before diagnosis.
Current sensor invalid	ACE fact invalid; operation blocked according to profile/safety policy.
Temperature sensor open/short	Invalid/unsafe fact; capability reduced or inhibited.
Bleed path ineffective	Service-ready blocked; fault recorded.
OUTPUT_FB mismatch	Output terminated or blocked; fault recorded.

27. Verification and Acceptance

Verification and Integration Ladder



Each rung requires recorded evidence before the next is released.

27.1 Evidence Package

- Released schematic, layout, wiring and mechanical drawings.
- ACE interface compliance matrix and signal polarity/default record.
- Selected component datasheets and derating calculations.
- Bank and output-loop characterization results.
- Gate timing, maximum-window and output-feedback measurements.
- OV, OC, thermal, interlock and wiring-loss fault-injection records.
- Analog scaling/calibration and validity-range records.
- Thermal rise and repetition-limit evidence.
- Pen insulation, strain-relief, cartridge and connector inspection results.
- Configuration, calibration and unresolved deviation register.

ID	Title	Requirement	Verification	Status
FS-VRF-001	Requirements traceability	Every frozen and proposed requirement shall have a verification method and recorded result before release.	Review	Frozen
FS-VRF-002	Logic first	ACE loopback, default-state and fault-path tests shall pass before a pulse bank is energized.	Test record	Frozen
FS-VRF-003	Progressive energy	Testing shall progress from unpowered to logic-level, low-energy, current-limited and instrumented pulse	Review/Test	Frozen

ID	Title	Requirement	Verification	Status
		stages with explicit release gates.		
FS-VRF-004	Independent cutoff proof	OV, OC, HW_INHIBIT and maximum-window cutoff shall each be demonstrated without relying on firmware diagnosis.	Fault injection	Frozen
FS-VRF-005	Command/actual proof	OUTPUT_FB shall be tested for correct response and mismatch detection across commanded and inhibited cases.	Timing test	Frozen
FS-VRF-006	Material coupon release	Workpiece trials shall begin only after dummy-load and instrumented output-path acceptance.	Review	Proposed

28. Integration Sequence

- Freeze this architecture and the ACE compatibility matrix.
- Build FS-800 interface conditioning and non-energized loopback fixtures.
- Implement FS-700 fault aggregation, source latch and independent maximum-window clamp using logic-level loads.
- Implement FS-100 feed-disconnect control and source telemetry without a pulse bank.
- Build the mechanical pen signal body, J-HND harness and dummy electrode cartridge.
- Select a conservative characterization bank and instrumented dummy load after open parameters are reviewed.
- Characterize FS-200 bank and residual-energy functions under current-limited bench conditions.
- Integrate FS-300 switch module and verify independent cutoff into a dummy load.
- Add FS-400 cable and FS-500 power cartridge; measure complete loop resistance and transient behaviour.
- Conduct material-coupon trials and freeze RevA operating limits, thresholds and BOM in Revision A.1.

BUILD ORDER: No step may require alteration of ACE. Any discovered mismatch is corrected in the Fusion Stage interface or raised as a formal master-baseline change request.

29. Open Requirements and Change Control

ID	Open decision	Required result	Closure evidence
OD-001	Reference material/joint envelope	PCB pad sizes, foil/contact thickness and materials.	Project decision + coupon plan
OD-002	Bank voltage range	Minimum practical voltage and maximum characterized voltage.	Characterization
OD-003	Stored-energy range	Minimum/maximum usable bank energy.	Characterization
OD-004	Pulse-duration range	Valid minimum/maximum commanded duration and clamp limit.	Instrumented testing
OD-005	Peak current envelope	Expected, maximum and trip threshold.	Dummy-load/material testing
OD-006	Repetition/cooldown	Allowed pulses per interval and thermal recovery rule.	Thermal testing
OD-007	Bench-source requirement	Voltage/current capability and grounding/isolation assumptions.	Source selection + test
OD-008	Output cable geometry	Length, resistance, flex and	Ergonomic + electrical test

ID	Open decision	Required result	Closure evidence
		termination.	
OD-009	Pen cartridge geometry	Tip material, spacing, projection, spring travel and retention.	Mechanical prototypes
OD-010	Connector subparts	Exact shell, keying, contacts and cable range.	Availability/enclosure review
OD-011	Sensor transfer functions	Divider, shunt/Hall range, NTC mounting and calibration.	Hardware selection
OD-012	Trip thresholds	OV, OC and thermal set points and hysteresis.	Failure envelope

Closure of an open decision shall update the requirements register, selected BOM, verification procedure and configuration record together. Silent changes to thresholds, connector assignments or ACE-facing behaviour are prohibited.

Appendix A. Requirements Register

This consolidated register is normative for the present working draft. Status remains Proposed or TBD until an approved revision freezes the item. Requirements marked Frozen derive directly from the ACE baseline or the agreed system boundary.

ID	Title	Requirement	Verification	Status
FS-GEN-001	ACE subordination	The Fusion Stage shall be subordinate to the frozen ACE architecture and shall not require changes to ACE hardware, pin allocation, connector function, signal ownership or firmware authority.	Inspection	Frozen
FS-GEN-002	Bench-fed RevA	RevA shall be powered from an external current-limited bench source; the source itself is not part of the Fusion Stage configuration item.	Inspection	Frozen
FS-GEN-003	No local controller	The Fusion Stage shall not include a second general-purpose controller that can independently authorize or schedule pulses.	Inspection/Test	Frozen
FS-GEN-004	Parameter freeze by evidence	Bank voltage, capacitance, pulse duration, peak current, repetition limit, thresholds and cable geometry shall be frozen only after documented characterization.	Review	Frozen
FS-CFG-001	No ACE redesign	Fusion Stage compliance shall be achieved entirely on the Fusion Stage side of the frozen interface.	Inspection	Frozen
FS-CFG-002	Historical concepts	Early boost-charged, dual-input, local-MCU and local-display concepts shall be treated as superseded background only.	Document review	Frozen
FS-CFG-003	Controlled deviations	Any deviation affecting ACE-facing signals, timing, polarity, ownership or segregation shall require a formal change request against the master baseline.	Review	Frozen
FS-MIS-001	Precision micro-bonding	The RevA reference configuration shall prioritize small, localized and instrumented joints over maximum energy or throughput.	Review/Demonstration	Proposed
FS-MIS-002	Modular characterization	The bank, switch, output cable and electrode cartridge shall be replaceable or reconfigurable without changing ACE contracts.	Inspection	Proposed
FS-BND-001	Raw-node segregation	Raw bank, busbar, switch, shunt,	Inspection	Frozen

ID	Title	Requirement	Verification	Status
		output and electrode nodes shall remain outside ACE and J-PWR/J-HND.		
FS-BND-002	Source boundary	The bench source shall connect through a defined input connector, protection path and ACE-controlled feed disconnect.	Inspection/Test	Proposed
FS-BND-003	Pen boundary	The pen shall present separate low-voltage signal and high-current power interfaces.	Inspection	Frozen
FS-ACE-001	Sole pulse authority	Only ACE PULSE_CMD may initiate conduction in the output switch stage.	Test	Frozen
FS-ACE-002	Dominant inhibit	Active HW_INHIBIT shall prevent or terminate gate drive regardless of PULSE_CMD state.	Fault injection	Frozen
FS-ACE-003	No trigger bypass	No electrical path from pen trigger or grip shall directly drive the Fusion Stage output switch.	Inspection/Test	Frozen
FS-ACE-004	No pulse memory	The Fusion Stage shall not store a pending pulse request after PULSE_CMD is removed.	Test	Frozen
FS-ACE-005	No autonomous retrigger	The Fusion Stage shall not generate repeated or extended pulses from a single ACE command.	Test	Frozen
FS-ACE-006	Open wiring safe	Open or disconnected ACE control wiring shall resolve to inhibited/unavailable states.	Fault injection	Frozen
FS-OPS-001	Charge/pulse exclusion	The bench-feed path shall be disconnected or otherwise proven non-conducting during the pulse window.	Test	Proposed
FS-OPS-002	Release required	The Fusion Stage shall support ACE enforcement of trigger release between operations and shall not self-repeat while trigger remains pressed.	System test	Frozen
FS-OPS-003	Post-pulse inhibit	The stage shall return to an inhibited state immediately after PULSE_CMD ends or any veto asserts.	Timing test	Frozen
FS-AUT-001	Fresh-edge dependence	The system shall not fire merely because TRIGGER_SW is already active when readiness, ARM or inhibit state changes.	System test	Frozen
FS-AUT-002	Veto monotonicity	A local failure or uncertain fact shall preserve or reduce authorization and shall never create conduction.	Fault injection	Frozen

ID	Title	Requirement	Verification	Status
FS-AUT-003	No OR authority	Local readiness, contact detection or hardware-valid signals shall not be ORed with PULSE_CMD to create gate drive.	Inspection	Frozen
FS-IF-001	Conditioned logic	Every external Fusion Stage signal presented to ACE shall be protected and conditioned for the ACE electrical domain.	Electrical test	Frozen
FS-IF-002	Connector protection	ESD, series impedance and filtering shall be placed at the harness entry appropriate to signal class.	Inspection/Test	Frozen
FS-IF-003	Return segregation	Shield/chassis, analog return, logic return and pulse-current return shall remain distinct until their defined bonding points.	Inspection	Frozen
FS-SRC-001	No direct pulsing from source	The bench source shall not be used as the direct workpiece pulse source.	Inspection/Test	Frozen
FS-SRC-002	Safe source loss	Loss of the bench source shall not create a gate pulse or defeat residual-energy control.	Fault injection	Frozen
FS-SRC-003	Polarity protection	The Fusion Stage input shall provide a defined response to reversed input polarity without creating an output pulse.	Test	Proposed
FS-IN-001	Input fuse/protection	The input path shall include protection sized from the characterized source, wiring and credible fault current.	Analysis/Test	TBD
FS-IN-002	Controlled disconnect	A hardware-controlled feed disconnect shall isolate the bank from the bench source when CHARGE_ENABLE is inactive.	Test	Proposed
FS-IN-003	Inhibit dominance	HW_INHIBIT and critical fault conditions shall force the feed disconnect safe independently of ACE software sequencing.	Fault injection	Frozen
FS-IN-004	Pulse exclusion	The feed path shall not conduct meaningful preparation current during the output pulse window.	Measurement	Proposed
FS-IN-005	Source telemetry	VIN_AUX and ICHG_MON shall be scaled, filtered and range-checked before ACE acquisition.	Calibration/Test	Frozen
FS-IN-006	Reverse-current behaviour	The selected feed-disconnect topology shall have documented reverse-current behaviour and shall not permit unintended bank backfeed.	Review/Test	TBD

ID	Title	Requirement	Verification	Status
FS-BANK-001	Voltage margin	Every bank component shall have rated and surge voltage margin above the characterized maximum bank voltage.	Design review	TBD
FS-BANK-002	Pulse suitability	Capacitors shall be selected using ESR, impedance, ripple, surge, lifetime and pulse-heating evidence, not capacitance and voltage alone.	Design review	TBD
FS-BANK-003	Assembled characterization	The assembled bank shall be measured for capacitance, effective series resistance, leakage, temperature rise and discharge repeatability.	Test	TBD
FS-BANK-004	Physical containment	Bank terminals and conductors shall be finger-safe behind tool-removable barriers in normal service states.	Inspection	Frozen
FS-BANK-005	Vent clearance	Capacitor pressure-relief vents shall not be obstructed or directed toward the operator or ACE electronics.	Inspection	Proposed
FS-BANK-006	No salvage assumption	Salvaged capacitors shall not be accepted into the released RevA configuration without measured health and traceable derating evidence.	Inspection/Test	Proposed
FS-BLD-001	Passive discharge	The bank shall have a passive residual-energy path effective after control-power loss.	Timing test	Frozen
FS-BLD-002	Active discharge	The active dump path shall be independently rated for the characterized bank voltage, energy and repetition.	Analysis/Test	TBD
FS-BLD-003	Confirmed safe voltage	Service access shall depend on measured VBANK below a frozen threshold, not elapsed time alone.	System test	Proposed
FS-BLD-004	Dump fault	Failure to observe the expected voltage decay after BLEED_ENABLE shall assert a fault or invalid state.	Fault injection	Proposed
FS-SW-001	Command dependence	Gate drive shall be impossible without active PULSE_CMD.	Inspection/Test	Frozen
FS-SW-002	Hardware enable chain	PULSE_CMD shall pass through hardware gating that includes HW_INHIBIT and independent trip/clamp vetoes.	Inspection/Test	Frozen
FS-SW-003	SOA-based selection	Switch devices shall be selected using safe-operating-area, transient thermal impedance, gate charge, temperature-	Design review	TBD

ID	Title	Requirement	Verification	Status
		dependent resistance and pulse repetition evidence.		
FS-SW-004	Parallel symmetry	If devices are paralleled, current path, gate impedance, thermal path and sensing shall be intentionally symmetrical.	Inspection/Measurement	TBD
FS-SW-005	Defined startup state	Gate-driver outputs shall be held off during power ramp, reset, disconnected input and undervoltage.	Test	Frozen
FS-SW-006	Output feedback	OUTPUT_FB shall report observed output conduction independently enough to detect command/actual mismatch.	Test	Frozen
FS-SW-007	Transient control	Voltage overshoot and ringing shall be measured at the assembled switch and output loop; suppression shall be selected from evidence.	Instrumented test	TBD
FS-CLP-001	Independent timing	Clamp timing shall not depend on the Nano Every timer, firmware loop, I2C, ADC or display.	Inspection/Test	Frozen
FS-CLP-002	Non-retriggerable	A stuck or repeated PULSE_CMD edge shall not extend the active maximum window.	Timing test	Frozen
FS-CLP-003	Characterized duration	The clamp limit shall be frozen only after the valid pulse envelope and worst-case switch cutoff are measured.	Review/Test	TBD
FS-CLP-004	Expiry fault	Clamp expiry shall terminate output and create a diagnosable fault source.	Fault injection	Frozen
FS-FLT-001	First action inhibit	Detailed diagnosis shall never be required before the hardware output path is inhibited.	Fault injection	Frozen
FS-FLT-002	Open-drain aggregate	FAULT_SUM shall use a conditioned aggregate method compatible with the frozen ACE direct input.	Electrical test	Frozen
FS-FLT-003	Source preservation	The source latch shall preserve fault detail until ACE requests reset after the source is absent.	Test	Frozen
FS-FLT-004	Reset cannot rearm	Clearing a latch shall not enable gate drive, restore preparation or create a pending pulse.	System test	Frozen
FS-FLT-005	Thermal policy	Critical thermal trips shall use independent thresholds where failure consequence requires immediate hardware cutoff.	Analysis/Test	TBD

ID	Title	Requirement	Verification	Status
FS-SNS-001	Conditioned range	All analog outputs shall remain inside the approved ACE ADC input range under normal and credible fault conditions.	Electrical test	Frozen
FS-SNS-002	Calibration	Each populated channel shall have a documented transfer function, calibration method and validity range.	Calibration review	TBD
FS-SNS-003	Trip independence	VBANK and IOUT_MON telemetry shall not be the sole implementation of TRIP_OV or TRIP_OC.	Inspection	Frozen
FS-SNS-004	Current sensor range	The output-current sensor shall not saturate or lose validity across the accepted pulse envelope without an explicit overrange indication.	Pulse test	TBD
FS-SNS-005	Snapshot coherence	Fusion Stage channel settling and update behaviour shall support coherent ACE TelemetrySnapshot acquisition.	System test	Proposed
FS-PTH-001	Loop characterization	The assembled output loop shall be measured or bounded for resistance, inductance, contact resistance and temperature rise.	Measurement	TBD
FS-PTH-002	Compact internal loop	Bank-to-switch and switch-to-output conductors shall be short, mechanically restrained and arranged to minimize loop area.	Inspection/Measurement	Proposed
FS-PTH-003	No solder-only pulse joint	Primary pulse-current joints shall not rely solely on ordinary solder for mechanical retention and current transfer.	Inspection	Proposed
FS-PTH-004	Dedicated connector	The pen power connector shall be physically incompatible with ACE signal connectors and shall provide positive retention.	Inspection	Frozen
FS-PTH-005	Source-side touch safety	The source-side output interface shall avoid exposed energized contacts in normal handling.	Inspection	Proposed
FS-PTH-006	Cable evidence	Cable selection shall use measured round-trip resistance, flex life, insulation temperature, bend radius and termination compatibility.	Design review/Test	TBD
FS-PTH-007	Strain relief	Both base and pen ends shall include strain relief that does not transfer bending load into electrical terminations.	Inspection	Proposed

ID	Title	Requirement	Verification	Status
FS-PEN-001	Separate harnesses	Pen signal functions and pulse-current conductors shall use separate connectors and electrically segregated paths.	Inspection	Frozen
FS-PEN-002	Trigger request only	The pen trigger shall connect only to the ACE conditioned input path and shall not switch pulse current or gate drive.	Inspection/Test	Frozen
FS-PEN-003	Grip fact	The grip switch shall provide an independent ACE fact and shall default safe on release or wiring loss.	Test	Frozen
FS-PEN-004	Replaceable cartridge	Electrode holders and tips shall be serviceable as a cartridge without disturbing the signal switch assembly.	Demonstration	Proposed
FS-PEN-005	Temperature sensing	THAND shall monitor a representative handpiece/electrode-mount temperature while remaining electrically isolated from the pulse path.	Calibration/Test	Proposed
FS-PEN-006	Operator insulation	The intended grip surface shall remain electrically insulated from the pulse-current path under normal use and single credible mechanical faults.	Inspection/Test	Proposed
FS-TOOL-001	Presence fact	HANDPIECE_PRESENT shall indicate a correctly connected signal harness and shall default absent on open wiring.	Test	Frozen
FS-TOOL-002	Tool ID	HANDPIECE_ID shall use a bounded resistor-coded or equivalent passive identification method compatible with the ACE analog channel.	Calibration/Test	Frozen
FS-TOOL-003	Contact-test energy	CONTACT_TEST shall use a separately limited, low-energy measurement path incapable of generating a Fusion pulse.	Analysis/Test	Proposed
FS-TOOL-004	No auto-fire	Valid contact-test results shall be facts for ACE and shall never initiate gate drive locally.	Inspection/Test	Frozen
FS-TOOL-005	Wrong-tool inhibit	Unknown, invalid or incompatible handpiece identity shall preserve inhibit until ACE policy resolves it.	System test	Proposed
FS-THM-001	Temperature limits	Maximum continuous and pulse-cycle temperatures shall be frozen for bank, switch, connector, cable and handpiece.	Review/Test	TBD

ID	Title	Requirement	Verification	Status
FS-THM-002	Cooldown fact	The Fusion Stage shall provide facts sufficient for ACE to enforce cooldown and repetition limits.	System test	Proposed
FS-THM-003	Fan failure	Where active cooling is required, loss of fan-good shall preserve or reduce authorization.	Fault injection	Proposed
FS-THM-004	No hidden hot spot	Acceptance testing shall include connector, cable termination, busbar joint and electrode-holder temperature inspection.	Thermal test	TBD
FS-MEC-001	Compartment segregation	The enclosure shall prevent pulse-current wiring and service tools from contacting ACE logic and signal wiring.	Inspection	Frozen
FS-MEC-002	Interlock	Opening the defined energized/service compartment shall assert the ACE enclosure interlock or equivalent dominant inhibit.	Test	Frozen
FS-MEC-003	Service proof	A service-safe condition shall require inhibit, feed disconnect, active/passive discharge and measured bank voltage below the frozen threshold.	Demonstration	Proposed
FS-MEC-004	Replaceable modules	Bank, switch and output harness modules shall be identifiable and replaceable without undocumented wiring changes.	Inspection	Proposed
FS-EMC-001	Loop-area control	Pulse-current forward and return paths shall be routed together to minimize magnetic loop area.	Inspection	Proposed
FS-EMC-002	Signal separation	J-PWR/J-HND wiring and analog sensing shall be separated from busbars, gate loops and output cable exits.	Inspection	Frozen
FS-EMC-003	Defined bonding	Chassis/shield, analog return, logic return and power return shall meet only at documented bonding points.	Inspection/Measurement	Frozen
FS-EMC-004	Connector protection	Protection components shall be located at harness entries rather than deep inside the board.	Inspection	Frozen
FS-EMC-005	Gate-loop control	Gate-driver supply, gate return and switching loops shall be compact and measured for ringing.	Inspection/Test	TBD
FS-EMC-006	Telemetry validity	Pulse activity shall not create undetected false-ready, false-trigger, false-presence or false-safe facts.	EMC/system test	Frozen

ID	Title	Requirement	Verification	Status
FS-DIAG-001	Non-energized diagnostics	Primary interface and fault-path verification shall be possible without an energized pulse bank.	Demonstration	Frozen
FS-DIAG-002	No service authorization	Service UART, diagnostic inputs and test points shall not become pulse authorization channels.	Inspection/Test	Frozen
FS-DIAG-003	Protected test points	Service test points shall expose conditioned or limited nodes; raw pulse nodes shall remain guarded.	Inspection	Proposed
FS-DIAG-004	Configuration record	Released hardware shall record board/module revision, sensor scaling, threshold set and populated options.	Review	Proposed
FS-REL-001	Safe single faults	A single foreseeable failure in control wiring, local logic supply, sensor wiring or gate-driver input shall not create an unauthorized pulse.	Fault analysis/Test	Frozen
FS-REL-002	No restart resume	Power restoration shall not resume preparation, authorization or an interrupted pulse.	Restart test	Frozen
FS-REL-003	Loss of advisory services	Failure of telemetry, fan status, contact test or identity services shall preserve or reduce authorization.	Fault injection	Frozen
FS-REL-004	Wear items	Electrodes, power contacts and flexible cable shall have inspection/replacement criteria based on measured degradation.	Service review	TBD
FS-VRF-001	Requirements traceability	Every frozen and proposed requirement shall have a verification method and recorded result before release.	Review	Frozen
FS-VRF-002	Logic first	ACE loopback, default-state and fault-path tests shall pass before a pulse bank is energized.	Test record	Frozen
FS-VRF-003	Progressive energy	Testing shall progress from unpowered to logic-level, low-energy, current-limited and instrumented pulse stages with explicit release gates.	Review/Test	Frozen
FS-VRF-004	Independent cutoff proof	OV, OC, HW_INHIBIT and maximum-window cutoff shall each be demonstrated without relying on firmware diagnosis.	Fault injection	Frozen
FS-VRF-005	Command/actual proof	OUTPUT_FB shall be tested for correct response and mismatch detection across commanded and inhibited cases.	Timing test	Frozen

ID	Title	Requirement	Verification	Status
FS-VRF-006	Material coupon release	Workpiece trials shall begin only after dummy-load and instrumented output-path acceptance.	Review	Proposed

Appendix B. ACE Signal Register

Signal	ACE pin/domain	Direction at ACE	Class	Fusion Stage responsibility	Safe/default meaning
FAULT_SUM	D2 direct	Input	A	Conditioned open-drain aggregate fault.	No-fault only when all required sources are valid.
TRIP_OV	D3 direct	Input	A	Independent bank overvoltage comparator.	Asserted/invalid blocks preparation and output.
ARM_SW	D4 direct	Input	A	Outside Fusion Stage; physical panel fact.	Open/unavailable is not armed.
HARD_SAFE_SW	D5 direct	Input	A	Outside Fusion Stage; dominant panel safe control.	Safe/inhibit dominates.
GRIP_SW	D6 direct	Input	A	Pen grip signal through J-HND conditioning.	Open is not enabled.
TRIGGER_SW	D7 direct	Input	A	Pen request signal through J-HND conditioning.	Open is no request.
OUTPUT_FB	D8 direct	Input	A	Observed output conduction state.	Inactive unless physical output observed.
PULSE_CMD	D9 direct	Output	A	Only positive pulse authorization input to Fusion Stage.	Inactive means no gate drive.
HW_INHIBIT	A0 direct	Output	A	Dominant hardware veto input.	Asserted on reset/unsafe state.
CHARGE_ENABLE	A1 direct	Output	B	Requests bench-feed connection for preparation.	Inactive on reset.
ENCLOSURE_INTLK	A2 direct	Input	A/B	Enclosure/service interlock fact.	Open/invalid inhibits.
HANDPIECE_PRESENT	A6 direct	Input	A/B	Pen signal-harness presence.	Open is absent.
TRIP_OC	A7 direct	Input	A	Independent output-current trip.	Asserted/invalid blocks output.

Appendix C. Telemetry Register

Channel	Name	Source	Purpose	Validity/fault expectations
AIN0	VBANK	Bank divider/buffer	Bank voltage and OV cross-check.	Open, short, overrange and stale detectable.

Channel	Name	Source	Purpose	Validity/fault expectations
AIN1	VIN_AUX	Bench input divider/buffer	Source presence and input voltage.	Open/reverse/out-of-range handled.
AIN2	ICHG_MON	Charge-current sense	Preparation current and feed diagnostics.	Zero offset, saturation and polarity characterized.
AIN3	IOUT_MON	Hall or shunt front end	Pulse-current waveform/result.	Bandwidth, range, saturation and pulse overload characterized.
AIN4	TBANK	NTC or equivalent	Bank thermal state.	Open/short and mounting lag characterized.
AIN5	TSTAGE	NTC or equivalent	Switch-stage thermal state.	Open/short and hot-spot relationship characterized.
AIN7	THAND	Insulated pen sensor	Handpiece/electrode-mount thermal state.	Electrical isolation and response time characterized.
AIN9	CONTACT_TEST	Limited measurement path	Continuity/contact quality.	Cannot generate Fusion pulse; open/short bounded.
AIN10	HANDPIECE_ID	Passive code network	Tool/cartridge identity.	Unknown and out-of-range distinguishable.
AIN11	VREF_MON	Reference monitor	ADC reference health.	Deviation invalidates affected telemetry.

Appendix D. Verification Matrix

ID	Verification	Pass condition	Evidence
V-01	ACE contract review	All Fusion signals match frozen direction, ownership and safe defaults.	Schematic/interface matrix
V-02	Unpowered inspection	Segregation, barriers, connector incompatibility, grounding and mechanical restraint.	Inspection record/photos
V-03	Default-state test	Reset, brownout, cable loss and local undervoltage produce inhibit.	Logic analyzer/test log
V-04	Trigger-path test	Pen button reaches ACE only; no direct gate path; pre-held trigger does not fire.	System test
V-05	Maximum-window test	Stuck PULSE_CMD is terminated by independent clamp.	Timing capture
V-06	OV fault injection	Independent comparator disables preparation/output and reports TRIP_OV.	Fault record
V-07	OC fault injection	Independent trip terminates output and reports TRIP_OC.	Fault record
V-08	OUTPUT_FB mismatch	Commanded/observed mismatch is detected and inhibited.	Timing capture
V-09	Bleed/dump test	Passive and active decay meet frozen thresholds; failure is detected.	Voltage-time record

ID	Verification	Pass condition	Evidence
V-10	Telemetry calibration	Transfer, validity, range and stale behaviour for each populated channel.	Calibration sheet
V-11	Loop characterization	Resistance, inductance, ringing and temperature of complete output loop.	Instrumented report
V-12	Thermal/repetition test	Bank, switch, connector, cable and pen remain within frozen limits.	Thermal report
V-13	Dummy-load pulse test	Pulse waveform, current, duration, cutoff and recovery.	Oscilloscope/current capture
V-14	Material-coupon trial	Reference joints meet quality and repeatability criteria.	Coupon record
V-15	Restart test	No restart restores preparation, armed state or pending output.	System test
V-16	Configuration audit	Hardware revision, thresholds, options, calibration and deviations recorded.	Release checklist

Appendix E. Source Register

ID	Source	Normative use
S1	NA-MASTER-001, NanoArc Master Technical Architecture and Configuration Baseline, RevA Freeze / Master Revision 1.2.	Highest-authority ACE system boundary, direct pin map, signal classes, connectors, telemetry, fault aggregation and configuration precedence.
S2	NA-CSHID-001, Control System and Human-Interface Architecture Manual, Revision A.1.	ACE authority model, HAL facts, timing, restart and machine-interface ownership.
S3	NA-ACEHW-001, ACE Hardware and Operator-Panel Architecture Manual, Revision A.1.	Direct safety inputs/outputs, connector register, machine I/O, analog channels and deferred decisions.
S4	pulse_welder_architecture.md, 2026-06-18.	Non-normative early mission, pen concepts and subsystem brainstorming.
S5	pulse_welder_parts_and_summary-3.md, 2026-06-18.	Non-normative historical parts and architecture ideas; superseded where inconsistent with ACE or RevA bench-fed scope.
S6	Project decisions through 2026-07-01.	Bench-fed RevA, ACE sole pulse authority, separate pen signal/power harnesses and Fusion Stage subordination to ACE.

END OF CONTROLLED DRAFT: Revision A.0 establishes architecture and requirements. Revision A.1 shall freeze the characterized operating envelope and procurement BOM without changing the ACE contract.